ABSTRACT OF THE DISCLOSURE

CHECK BIT FREE ERROR CORRECTION FOR SLEEP MODE DATA RETENTION

A DRAM memory has a reduced refresh rate in a sleep mode to conserve power. Error Correction Codes (ECC) are used to correct errors that may arise due to the reduced refresh rate. ECC encoding occurs at the time of entering the sleep mode and ECC decoding for error detection and correction need only take place upon wake up when resuming active mode. In addition, the memory system reassigns a portion of the memory for storing the additional parity bits required for the error correcting code (ECC).